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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,025	10/10/2001	Jung-Lim Yoon	SAM-0260	7520

7590

08/26/2003

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EXAMINER

PAREKH, NITIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/974,025

Applicant(s)

YOON ET AL.

Examiner

Nitin Parekh

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— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 6-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greer (US Pat. 6451681).

Regarding claim 1, Greer discloses a flip chip type semiconductor device having pad and fuse areas (not numerically referenced –see device/pad area and peripheral fuse area in left and right side of the broken line respectively in Fig. 8; Col. 6, line 55- Col. 7, line 15) comprising:

- an interlayer insulation layer/IIL (116 in Fig. 8) formed on a semiconductor substrate (100 in Fig. 8)
- an insulating dielectric layer (118 in Fig. 8) formed on the IIL in a region/given region in pad and fuse areas
- a first metal line (124 in Fig. 8; Col. 3, line 4 and 15) formed in the region of the insulating layer having the pad area
- a second metal line (124 in Fig. 8; Col. 7, line 15-37) formed in the region of the insulating dielectric layer having the fuse area

- a fuse (802 in Fig. 8) covering the second metal line and a portion of the insulating dielectric underneath, the fuse being formed of an aluminum (Col. 7, line 28), the material being the same material as that of the pad, and
- a layer comprising a polyimide (706 in Fig. 8; Col. 7, line 8) covering the whole surface of the substrate including the fuse

(Fig. 8; Col. 6, line 52- Col. 8, line 38; Col. 3-5).

Greer fails to teach:

- a) the insulating dielectric layer being a passivation layer
- b) a pair of second metal lines being formed in the fuse area, and
- c) an under-bump metal layer (UBML) pattern and a bump sequentially stacked on an exposed pad covering a portion of the first metal line, the pad being exposed through an opening in the polyimide layer covering the whole surface of the substrate

a) Greer further teaches in an embodiment of Fig. 3, the layer serving as the passivation layer (300 in Fig. 3) being made of conventional insulating dielectric material comprising silicon oxynitride, plasma enhanced nitride or their combination to provide an improved diffusion barrier (Col. 4, lines 25-27; Col. 5, lines 48-51).

b) Greer further teaches in an embodiment of Fig. 7, the fuse (702 in Fig. 7) covering a pair of second metal lines (124 in Fig. 7) and the insulating dielectric layer there between (Col. 6, line 52- Col. 7, line 15).

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c) Greer further teaches in the embodiment of Fig. 3, an under-bump metal layer (UBML) pattern and a bump (314 and 310 in Fig. 3; Col. 4, line 37- 65) being sequentially stacked on an exposed aluminum pad (202 in Fig. 3; Col. 3, line 63; Col. 7, line 10- see) covering a portion of the first metal line to form a flip chip device (Col. 5, line 5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first and second metal lines being formed in the passivation layer and the UBML pattern and a bump being sequentially stacked on the exposed pad as taught by Greer in the embodiment of Fig. 3 and the pair of second metal lines being formed in the fuse area as taught by Greer in the embodiment of Fig. 7 so that diffusion barrier and insulation can be improved in Greer's device.

----- Regarding claims 3 and 4, Greer teaches substantially the entire claimed structure as -----
applied to claim 1 above, including the first and second metal lines/patterns including a copper layer (124 in Fig. 8) and a diffusion metal layer/pattern such as tantalum nitride (122 in Fig. 8) enclosing sidewalls and bottoms of copper layer (Col. 3, line 15; Col. 3, line 55).

Regarding claim 5, Greer teaches substantially the entire claimed structure as applied to claim 1 above, including the pad and the fuse including a barrier/adhesion layer and

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an aluminum layer/pattern being stacked in order (200/202 and 700/702 in Fig. 3 and 7/8 respectively; Col. 3, line 35-65; Col. 6, line 55- Col. 7, line 15).

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable Greer (US Pat. 6451681) in view of an admitted prior art (APA).

Regarding claim 2, Greer discloses substantially the entire claimed structure as applied to claim 1 above, but fails to specify the passivation layer including a lower silicon nitride, an intermediate silicon oxide and an upper silicon nitride being stacked in order.

APA teaches using the passivation layer including a lower silicon nitride, an intermediate silicon oxide and an upper silicon nitride (13/15/17 in Fig. 1) being stacked in order to provide an improved diffusion barrier and insulation for the device (see specification pages 1-3).

~~It would have been obvious to a person of ordinary skill in the art at the time~~
invention was made to incorporate the passivation layer including a lower silicon nitride, an intermediate silicon oxide and an upper silicon nitride being stacked in order as taught by APA so that diffusion barrier and insulation can be improved in Greer's device.

R s p o n s t o A r g u m e n t s

4. Applicant's arguments filed on 06-16-03 have been fully considered but they are not persuasive.

A. Applicant contends that Greer teaches forming the first and second metal lines in the insulating dielectric layer and not in the passivation layer.

However, as explained above, Greer further teaches the layers serving as the passivation layer and the dielectric layer being made of same material being used as conventional dielectrics including silicon oxynitride, plasma enhanced nitride or their combination (Col. 4, lines 25-27; Col. 5, lines 48-51).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

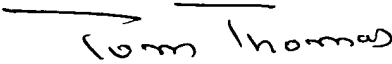
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
08-15-03


TOM THOMAS
SUPERVISORY PATENT EXAMINER
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